VIDEO DISPLAY AND 24K MEMORY SYSTEM

User Reference Guide

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ABSTRACT

This document describes the features of the Video Display and Memory system for TERAK Model 8510A data processor systems. Display formats and control are presented. Detail for programming use is also included.

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1.0 SCOPE

This document describes the features and specifications of the video display and memory system for the TERAK Model 8510/a GRAPHICS COMPUTER SYSTEM. It is the controlling document for hardware/software interface definitions and programming characteristics.

2.0 INTRODUCTION

The display and memory system provides the 8510/a with main memory and an extensive display capability. This system occupies a single 8-½" x 10" PWB slot on the system backplane. Output from the system drives a video display using a raster scan dot matrix. Programs can display both graphics and characters from independent buffers. In addition, the dot pattern displayed for any valid character code may be changed by program control of the alterable character generator. Features of the system include:

- 24K word memory - Combined with the 4K word memory on the 8510/a processor, a total of 28K 16-bit words is provided.

- 320 dot wide by 240 dot high graphics display. This dot matrix is compatible with medium-resolution, low cost video monitors. An aspect ratio of .75 maintains a "comfortable" viewing area.

- Square dot matrix graphic display. Horizontal and vertical dot spacing are equal, eliminating any need for scaling correction.

- Main Memory graphics display buffer. The graphics display is refreshed directly from the main memory. The buffer start address is under program control, accommodating variable boundaires between programs and buffers, simplifying addressing, and allowing rapid switching between dual buffers.

- Zone blanking of the graphics and character display. By selectively blanking unused zones of the graphics display, memory is released for use as a program and data storage area.

- 2-port memory structure. Graphics display refresh does not use the 8510/a central data bus. Data processing can continue at essentially full speed during graphics display.

- 24 x 80 character display, 25 x 80 character storage. Characters can be displayed simultaneously with graphics. Graphics and character display dot matrices are overlaid, and coincident. Graphics and character displays, when overlayed, are visually distinct.

- Display "panning" *and* "scrolling" - in addition to normal display scrolling, the 25th line of the page buffer (hidden line) allows changing one row without disturbing the other 24 rows (lines). This permits panning of display in a continuous motion.

- 8 dot wide by 10 dot high adjacent character blocks. Accommodates 5 x 7 characters with lower case descenders. Also 7 x 9 characters and special graphics characters can be displayed.

- Page buffer independent of main memory buffer is both read and write, facilitating editing the character display.

- 192 character code set. Full 8 bit byte used.

- Writeable character generator. By program modification of the generator buffer, any 8 x 10 dot pattern can be displayed for any of the 192 character codes. Foreign languages, APL, and "primitive graphics" (e.g. histograms or forms) are easily supported under program control.

- Keyboard input. The video controller inputs data from a keyboard thru the standard control console address or is switch selectable to alternate addresses.

- Control Console operation. Hardware is provided to allow full control console input and output. In this mode, the video display is equivalent to a "glass teletype" without requiring an additional serial interface for standard system console operation.

3.0 MEMORY

The memory and display system provides the 8510/a with 24K 16-bit words of dynamic Read-Write memory. The memory occupies banks 1 thru 6 (addresses 20000 to 160000) of the processor address space. The memory cycles at full bus speed when the graphics display is blanked, and is functionally independent of the video controller.

4.0 VIDEO CONTROLLER

The video controller is designed to provide medium resolution graphics and random-addressed character displays on the video terminal. Both displays are refreshed at 60 frames per second. The 24K memory is structured in a two-port design allowing access by both the processor and video controller (graphic display portion). This allows essentially full processor speed while the displays are being refreshed. The character display is refreshed simultaneously with the graphics display. Otherwise, the graphics display and character display are independent.

The graphics display is presented on the video display device as a matrix of dot positions, 320 wide by 240 high. This area is presented with an aspect ratio of .75 such that there is equal spacing between any two adjacent dot positions. This "square array" minimizes the computation requirements for accurate placement of graphics. When active, the graphics display illuminates or blanks each dot according to the contents of a buffer in the memory. This buffer can be viewed as a matrix of 240 lines of 20 words each.

Each line holds a total of 320 bits, which are mapped onto the 320 dots of one line of the graphic display. Maximum memory requirements are 4800 words for this buffer. This can be reduced, with simultaneous reduction of the area of the graphics display, by the selective blanking feature.

The character display is presented on the video display device as a 640 wide by 240 high matrix of dot positions. The horizontal dot spacing is one-half the vertical. Alternate horizontal dot positions are coincident with the graphics display matrix, such that the same area is displayed. Each character is displayed within an 8 dot wide by 10 dot high block, as shown in Figure 1, allowing display of a total of 1920 characters simultaneously with the graphics display. Each character position is illuminated according to the contents of the page buffer, and the contents of the character generator memory. The page buffer is a randomly addressable 2K byte, read-write memory independent of main memory.

Both the graphics display and character display can be selectively blanked. For blanking control, the display matrix is divided into three horizontal zones: 80 lines by 320 dots each for the graphics display, or 8 rows of 80 character blocks each for the character display. Each zone may be selectively blanked or displayed. Blanking of any one character display zone is mutually independent of the blanking of any one graphics display zone. When a graphics display zone is blanked, the corresponding area of the graphics display buffer in main memory is not read during refresh, thus reducing buffer storage size. If all zones of the graphics display buffer are blanked, no graphics refresh occurs.

The character display page buffer is structured in a two-port manner, similar to that of the graphics display, thus allowing simultaneous refresh of graphics and character displays. This is possible since the page buffer is completely independent from main memory. The page buffer is organized as 25 rows of 80 characters each. 24 rows of the page buffer, starting at the row number held in the Video Index Register (VIR), are displayed on the video display device, after translation by the character generator. The 25th row of the page buffer is provided to allow continuous panning of the display by stepping the VIR. The 25th row is never displayed in whole. As shown in Figure 1, each byte of the page buffer is translated into a 8 by 10 dot matrix by the character generator. The character generator is controlled by the generator buffer which is separate from main memory and the page buffer. It holds 192 blocks of dot patterns, corresponding to 192 valid 8 bit codes. The contents of the character generator buffer are established by the operating system or the user before characters can be displayed. Any special characters or character sets can be used by writing patterns into the generator buffer.

The generator buffer is both read and write memory, allowing easy generation of video reverse and modified characters. Since the page buffer is also both read and write memory, it can be used for direct storage of the text under attention, without need for a second image in main memory.

The video controller is also capable of generating audible sounds at the display device. (See 11.0)

5.0 GRAPHICS DISPLAY

The graphics display is presented as a 320 dot wide by 240 line matrix, mapped from a 4800 word memory area of 240 lines of 20 words. The starting address of the single graphics display block must be on a word boundary (even) and loaded into the graphics address register. The area from which the graphics display is to be refreshed will be any or all of the three 1600 word zones starting at the address in the address register and selected by the graphics zone blanking bits in the video control register. If a zone is thus blanked by the control register blanking bit, the corresponding 1600 word memory area will not be read during refresh.

If zones are blanked, the address register must still contain a starting address as if all three zones were being displayed. Any zones that are not blanked by the control register blanking bit, must correspond to a buffer within the 24K word area of banks 1 thru 6, and may not be in banks 0 (addresses 0 to 20000) or 7 (160000 and up). Note that blanked zones may be partially or completely within banks 0 or 7. However, un-blanking such zones will cause unpredictable results.

Access to memory by the video controller to refresh the graphics display results in a worst-case processor thruput degradation of approximately 20%. Typical degradation is less than 5%. The degradation decreases as the graphics display zones are blanked. No degradation occurs if all three zones are blanked.

6.0 CHARACTER DISPLAY

The character display presents a 640 dot wide by 240 line matrix, with alternate dots mapped coincident with the graphics display matrix. The character display matrix is divided into 24 rows of 80 character blocks each, as shown in Figure 1. Each block is an 8 dot wide by 10 line high area in which one character is displayed after translation by the character generator. The contents of the character display is refreshed from the page buffer simultaneously with the refresh of the graphics display from main memory.

The character page buffer is a 2K byte memory independent of the main memory. This 2K byte memory is mapped onto 4K bytes of address space, starting at address 160000 in the I/O address area. Figure 2 describes the mapping technique.

To address the page buffer, bit 7 of the Video Control Register (VCR) must first be cleared to a zero. The contents of the page buffer can be read as well as written, however, only byte addressing may be used. Columns are addressed left to right as 0 thru 117_8. Rows are addressed top to bottom as 0 thru 30_8. At each location within the mapped matrix, one 8-bit byte is stored. The byte code must be 40_8 thru 177_8 or 240_8 thru 377_8. During refresh of the character display, all bytes are translated by the character generator using the generator buffer and, when within an unblanked zone, are displayed on the rows and columns of the video display device.

The absolute position of a character on the video display device is determined by 1) its position in the page buffer (see Figure 2), and 2) the contents of the video index register (see Figure 3). This provides a hardware scrolling capability. Column position is not affected by the VIR. The row position is indexed by the upper byte of the VIR. Thus, to place a character at absolute row R of the display, while the upper byte of the VIR contains an index value r, it is necessary to address row R + r, modulo 24, of the page buffer, (Note: rows count from 0)

The low byte of the VIR indexes the starting scan line of the display. When this byte of the VIR is non-zero, portions of two rows of characters (e.g. rows 0 and 24) are displayed. Using this feature, the display may be "panned" in a continuous motion, as well as "scrolled" by the upper byte of the VIR. The 25th row (hidden row) of the page buffer allows changing one row of the buffer without disturbing the 24 other rows being displayed. The VIR can only be addressed as a word.

The generator buffer is a 2K byte memory independent of both main memory and of the page buffer. This 2K byte memory is mapped onto 4K bytes of address space starting at address 160000 in the I/O address area. Figure 4 describes the mapping technique.

To address the generator buffer, bit 7 of the VCR must first be set to a one. The contents of the generator buffer can be read as well as written, however, only byte addressing may be used. The bytes within the generator buffer are addressed by character code and scan line. Character codes must be only 40_8 thru 177_8 or 240_8 thru 377_8. Scan lines are addressed top to bottom (with respect to the 8 dot wide by 10 dot high block to be displayed for a given character code) as 0 thru 11_8. Bits 0 thru 7 of each byte thus addressed correspond to the dots of the addressed scan line from left to right.

7.0 CONTROL

Figure 5 illustrates the Video Control Register (VCR). All bits are indeterminate on power-up or system reset. Figure 6 illustrates the Graphics Address Register (GAR). The 16-bit graphics buffer address is written into the GAR as one word.

8.0 SYNCHRONIZATION

The display refresh of both graphics and characters is synchronized with the event clock such that an interrupt will occur at the end of the display refresh (start of the vertical retrace period). This allows software to synchronize changes in the graphics and character displays, so that changes occur between display frames (refresh cycles).

9.0 KEYBOARD INPUT

The video display controller supports keyboard input. Data from the keyboard will be input through a register pair, shown in Figures 7 and 8. The DONE bit in the Keyboard Status Register (KSR) will be set, and (if the interrupt enable is set) an interrupt through vector 60 will be requested, when a key is stroked. The data is then available in the Keyboard Data Register (KDR), and may be read multiple times until the next keystroke occurs. The DONE bit will be cleared by the first read of the KDR after the DONE bit was set. The keyboard address may be switched to an alternate set, as summarized in Figure 12.

10.0 CONSOLE PRINTER EMULATOR

Normally, the control console is assumed to have a serial printer which "scrolls" its display. Since the character display is a random-addressable, indexed fixed page. software is required to emulate the console printer, and hardware is provided to capture the serial output of characters.

The Emulator Status Register (ESR) and Emulator Data Buffer (EDB) are provided by the video controller to support emulation of the control console device. Figures 9 and 10 illustrate the register pair. When data is written into the EDB, the DONE bit in the ESR is cleared. The data will remain captured in the EDB and is available for software to emulate the console output device by typically transferring the byte into the page buffer. The ESR DONE bit is set when the EDB is read by the emulator software. If the interrupt enable bit in the ESR is set, an interrupt will be requested thru vector 64 approximately 480 microseconds after the ESR DONE bit is set. An interrupt thru vector 164 will be requested immediately when the DONE bit is cleared, independent of the interrupt enable bit. The EDB may also be read and written at address EDBA (Figure 11) without affecting the DONE bit or interrupt conditions. The emulator addresses may be switched to an alternate set, as summarized in Figure 12.

11.0 AUDIO ALARM

The video control register supports an audible device located in the video display unit. There are two modes of operation: continuous tone and software generated tone, controlled by two bits in the VCR (Figure 5). Bit 11, when set, generates a continuous 780 Hz tone. Bit 8 drives an A.C. coupled D/A converter. Frequency of the tone generated by bit 8 is determined by the rate at which it is written on or off.

12.0 VIDEO CONTROLLER SOFTWARE SUPPORT

The RT-11/85A operating system and its language processors use the character display as a console display by means of the emulator status and data registers. The VT .SYS system handler receives data from the emulator hardware, and emulates a "glass teletype" through control of the page buffer. The console keyboard input is supported by RT-11/85A also. A utility program, VTBOOT.SAV, supplied with RT-11/85A will modify the standard bootstrap to cause, at bootstrap time:

1) automatic writing of the generator buffer with standard ASCII character patterns, and

2) a permanent load of the VT. SYS handler to emulate the console output device.

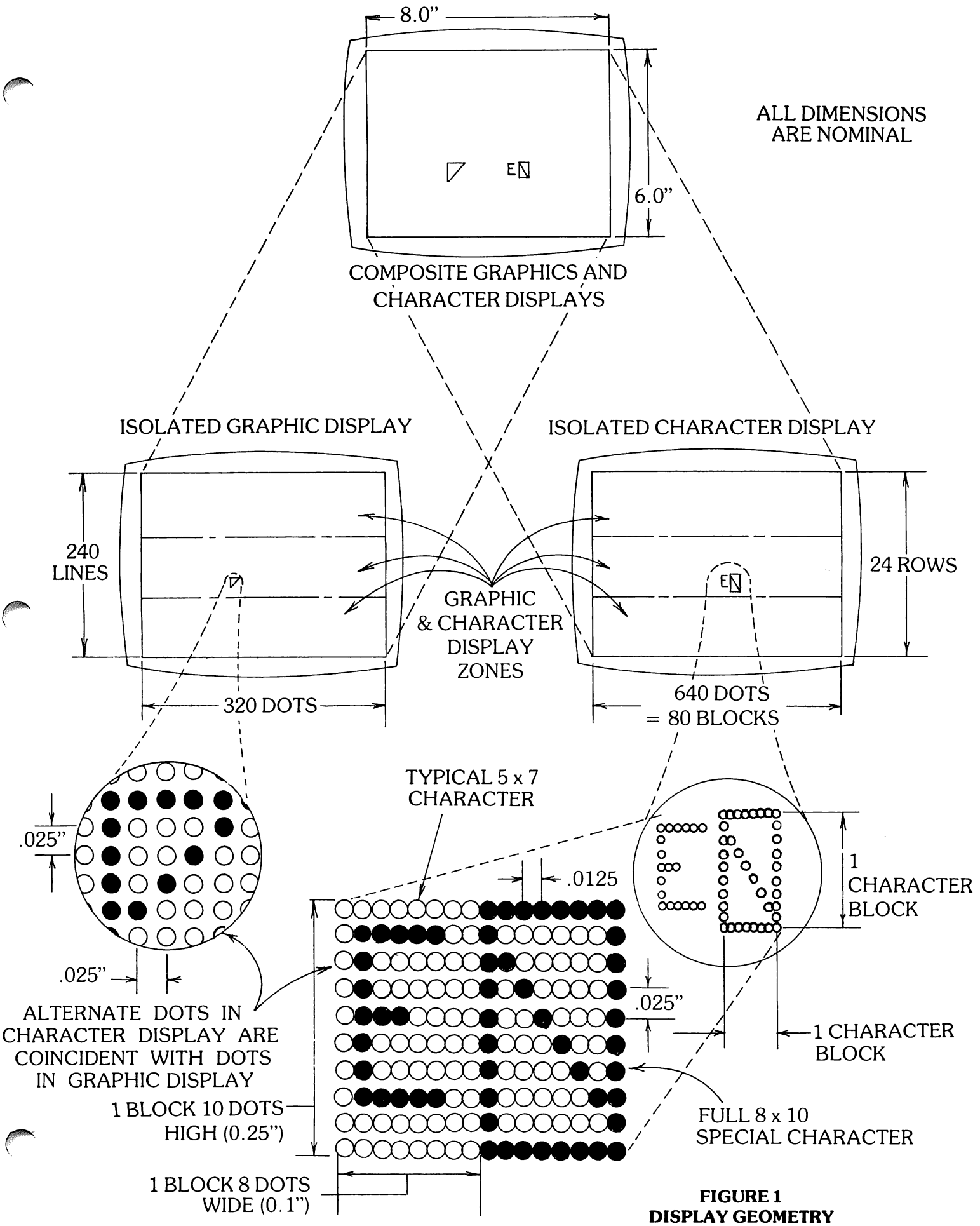
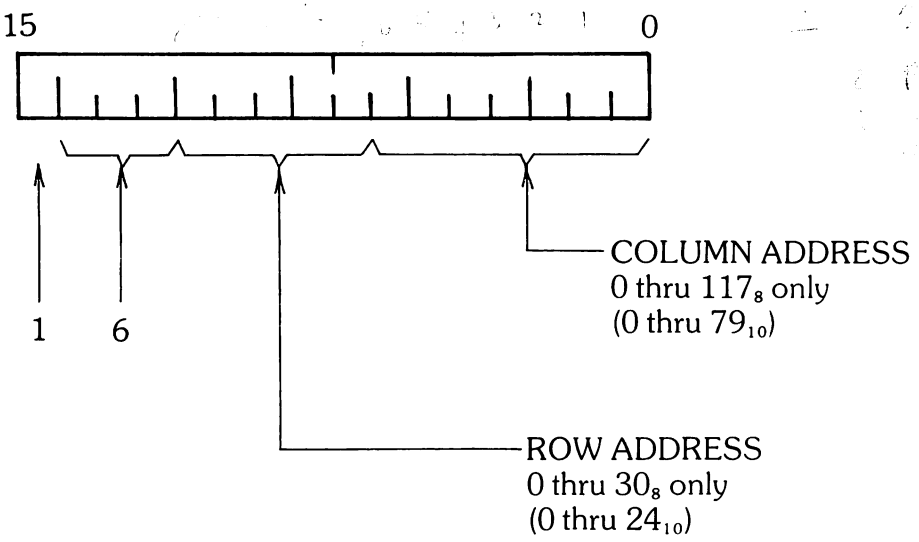


FIGURE 1
DISPLAY GEOMETRY

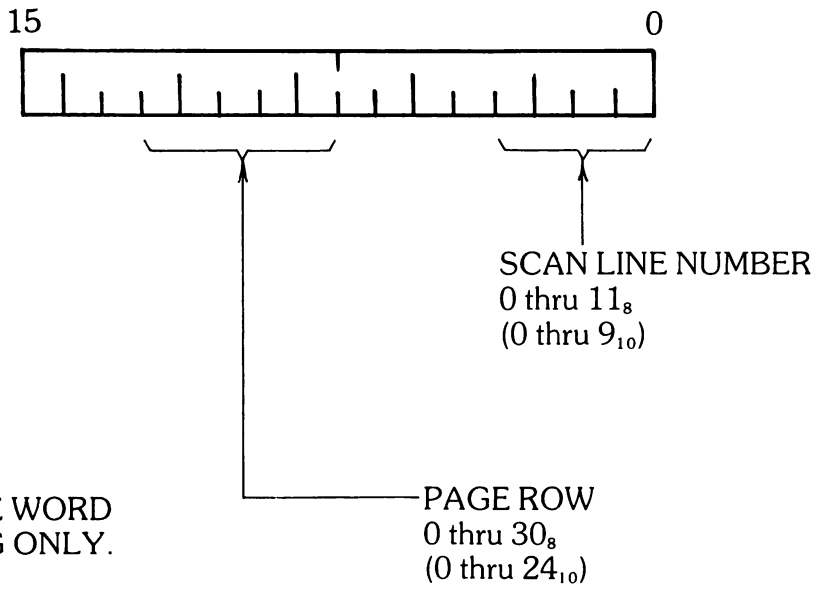
160000 - 167777



NOTE: ROW ADDRESSES ARE
INDEXED BY THE VIR
TO ABSOLUTE ROW POSITION

PAGE BUFFER ADDRESS MAP
FIGURE 2

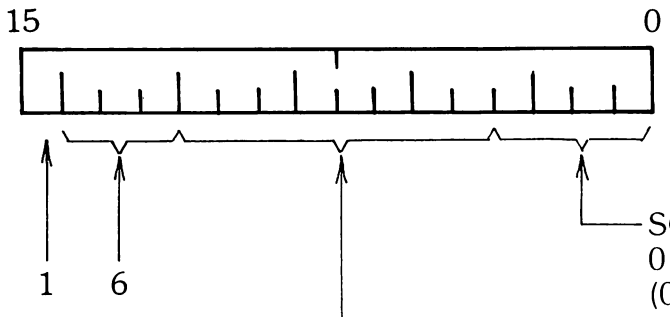
VIR 177742



NOTE: READ/WRITE WORD
ADDRESSING ONLY.

VIDEO INDEX REGISTER (VIR)
FIGURE 3

160000 - 167777



NOTE: WITHIN EACH BYTE ADDRESSED PER THIS MAP, ONE DOT ROW IS REPRESENTED. LSB (BIT 0) OF DATABYTE CORRESPONDS TO LEFTMOST DOT OF THE DISPLAYED ROW. MSB (BIT 7) CORRESPONDS TO RIGHTMOST DOT OF THE ROW, ALL OTHER BITS/DOTS MAPPED ACCORDINGLY.

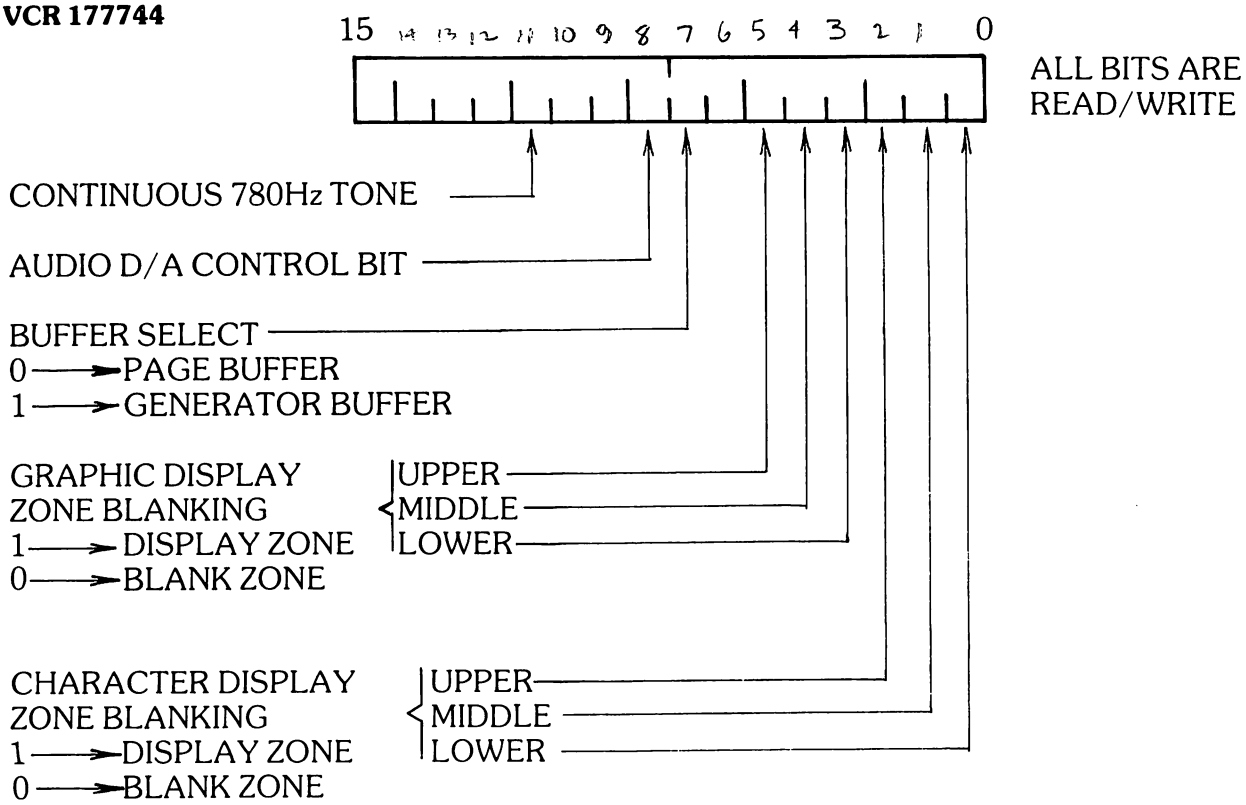
8 BIT CHARACTER CODE
40_8 thru 177_8 and
240_8 thru 377_8 only

40_8 thru 177_8 corresponds to standard ASC11 character codes

GENERATOR BUFFER ADDRESS MAP

FIGURE 4

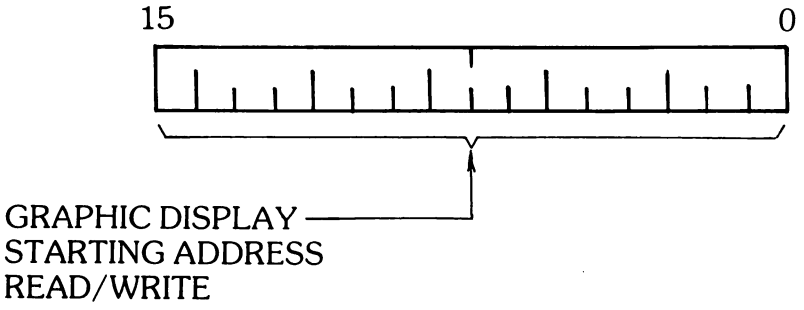
VCR 177744



VIDEO CONTROL REGISTER (VCR)

FIGURE 5

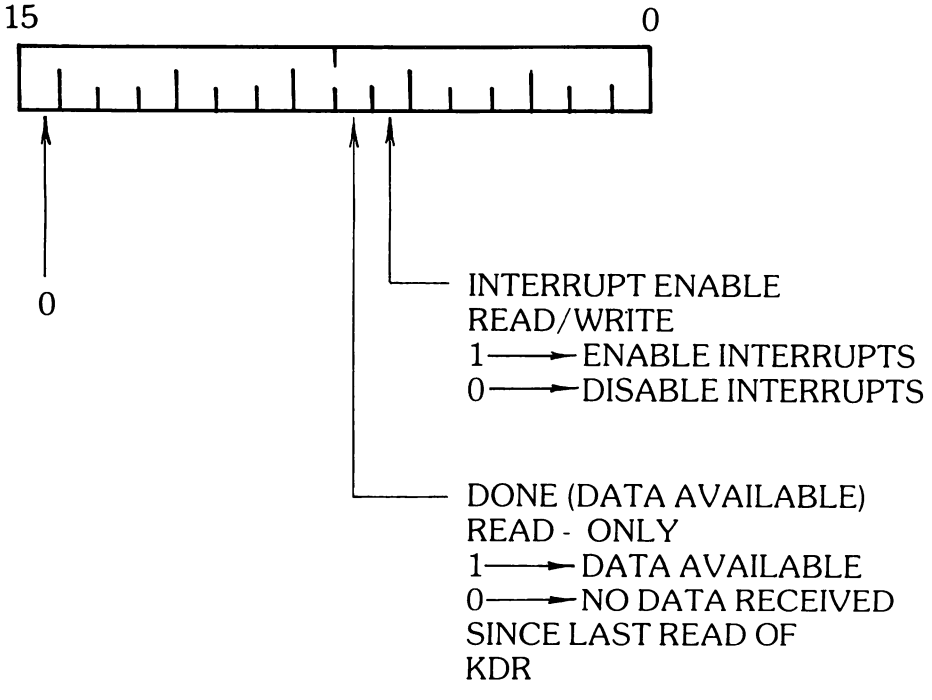
GAR 177740



GRAPHIC ADDRESS REGISTER (GAR)

FIGURE 6

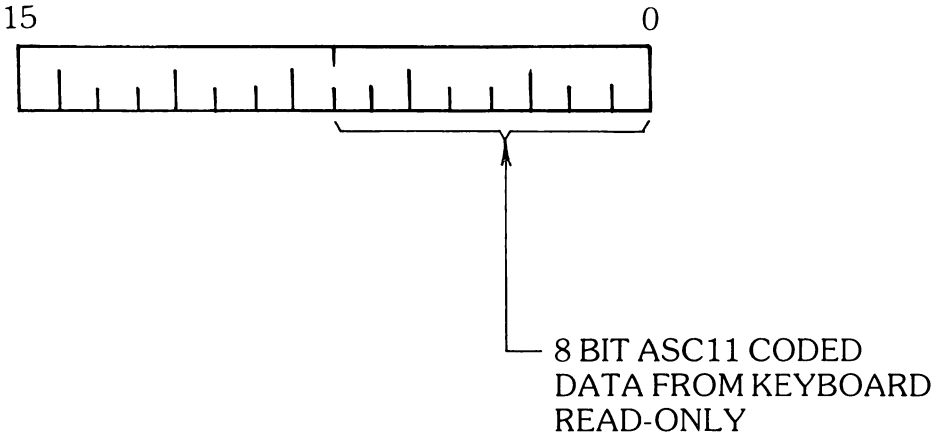
KSR 177560



KEYBOARD STATUS REGISTER (KSR)

FIGURE 7

KDR 177562

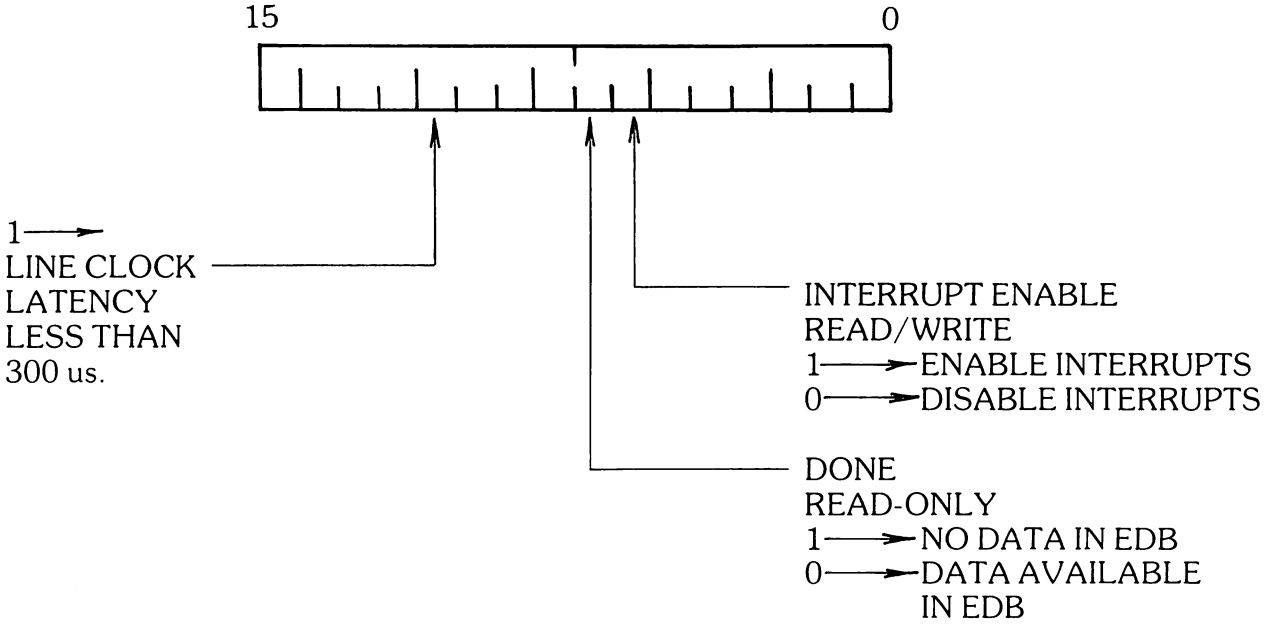


NOTE: KSR DONE BIT
IS CLEARED BY
READING THE KDR

KEYBOARD DATA REGISTER (KDR)

FIGURE 8

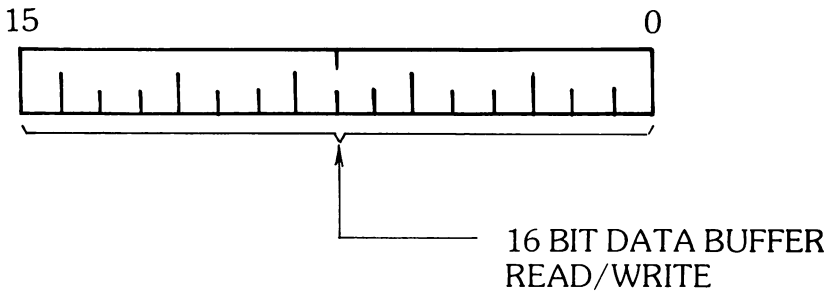
ESR 177564



EMULATOR STATUS REGISTER (ESR)

FIGURE 9

EDB 177566

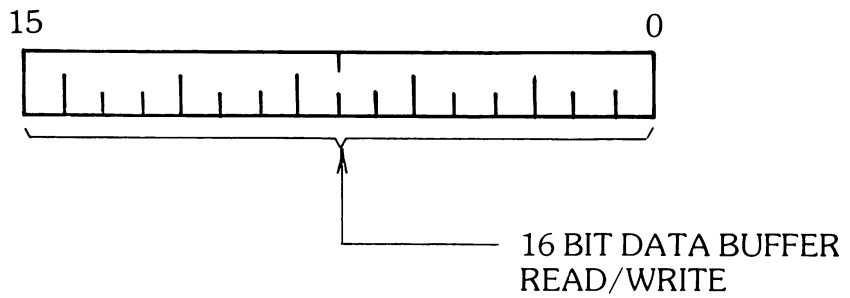


NOTE: ESR DONE BIT
IS SET BY READING
THE EDB AND IS
CLEARED BY WRITING
DATA INTO THE EDB

EMULATOR DATA BUFFER (EDB)

FIGURE 10

EDBA 177746



NOTE: THE EMULATOR DATA
BUFFER CAN BE READ
AND WRITTEN AT THIS
ADDRESS WITHOUT
AFFECTING THE STATE OF
THE DONE BIT IN THE ESR.

EMULATOR DATA BUFFER, ALTERNATE

FIGURE 11

REGISTER	ALTERNATE ADDRESS SWITCH OFF	ON
KSR	177560	177760
KDR	177562	177762
KSR VECTOR	60	70
EDR	177564	177764
EDB	177566	177766
EDR VECTORS	64/164	74/174
EDBA	177746	177746
GAR	177740	177740
VCR	177744	177744
VIR	177742	177742

REGISTER ADDRESS SUMMARY

FIGURE 12