terak
CORPORATION

ASYNCHRONOUS SERIAL INTERFACE
PROGRAMMING AND USE

ABSTRACT

This document describes the features of the Asynchronous Serial Interface for TERAK Model 8510 data processor systems. Cable wire lists and switch settings are presented. Detail for programming use is also included.

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REV D

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NOTES ON PROGRAMMING AND USE OF THE 8510 SERIAL INTERFACE

THE STANDARD SERIAL INTERFACE FOR 8510 AND 8510A SYSTEMS SUPPORTS ELECTRICAL CONNECTION IN ONE OF THREE MODES: 20 MA CURRENT LOOP, RS-232C AS DATA TERMINAL EQUIPMENT, AND RS-232C AS DATA COMMUNICATION EQUIPMENT. ONLY ONE OF THESE CONNECTIONS CAN BE MADE AT A TIME. ALL CONNECTIONS AND CONTROL OF THE SERIAL INTERFACE ARE ON THE SERIAL EIB (EXTERNAL INTERFACE BOARD), REPRESENTED SCHEMATICALLY BELOW. THERE ARE THREE CONNECTORS AND SIXTEEN SWITCHES. CONNECTOR J1 IS USED FOR RS-232C INTERFACE USING THE SERIAL INTERFACE AS DATA COMMUNICATIONS EQUIPMENT. CONNECTOR J2 IS USED FOR RS-232C INTERFACE USING THE SERIAL INTERFACE AS DATA TERMINAL EQUIPMENT. CONNECTOR J3 IS USED FOR CURRENT LOOP INTERFACE, AND ALSO FOR RS-232C INTERFACE AS DATA COMMUNICATIONS EQUIPMENT. THIS LATER OPTION (RS-232C CONNECTION THRU J3) ALLOWS USE OF A SIMPLER CONNECTOR (NYLON SHELL TYPE) FOR RS-232C CONNECTION. THE SIXTEEN SWITCHES ON THE SERIAL EIB (S1 & S2) CONTROL ADDRESSING AND CHARACTERISTICS OF THE SERIAL INTERFACE.

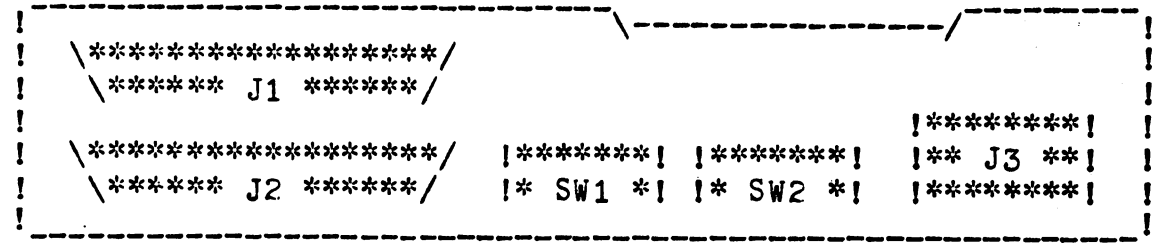

FIGURE 1 SERIAL EIB LEGEND

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;       THIS DOCUMENT ASSUMES FAMILIARITY WITH ANSI SPECIFICATION
;       RS-232C FOR DATA COMMUNICATIONS, AND ALSO WITH CURRENT LOOP
;       INTERFACE TECHNIQUES. DETAILED SIGNAL DESCRIPTIONS
;       WILL NOT BE PRESENTED HERE. THE READER IS REFERED TO:
;       "TECHNICAL ASPECTS OF DATA COMMUNICATION" MCNAMARA,DEC.
;
;-----------------------------------------------

;       RS-232C PIN ASSIGNMENTS AND SIGNAL DEFINITIONS CONFORM
;       TO THE ANSI STANDARD. THEY ARE PLACED HERE FOR REFERENCE.
;
;-----------------------------------------------

;       PIN LIST, RS-232C CONNECTION AS DATA COMMUNICATIONS EQUIPMENT. (DCE)
;       ALL CONNECTIONS TO J1, NO CONNECTIONS ALLOWED TO J2 OR J3.
;       USE THE FOLLOWING PARTS, OR EQUIVALENT IN THE CABLE ASSEMBLY:
;               CONNECTOR, MALE 232 PLUG        CINCH #  DB 25P
;               SHELL, PLUG                     CINCH #  DB 5126-1
;
;       PIN #   SIGNAL NAME                     IN/OUT
;
;       J1 - 1  FRAME GROUND
;       J1 - 7  SIGNAL GROUND
;       J1 - 8  CARRIER DETECT                  OUTPUT
;       J1 - 4  REQUEST TO SEND                 INPUT
;       J1 - 3  RECEIVE DATA                    OUTPUT
;       J1 - 20 DATA TERMINAL READY             INPUT
;       J1 - 5  CLEAR TO SEND                   OUTPUT
;       J1 - 6  DATA SET READY                  OUTPUT
;       J1 - 2  TRANSMIT DATA                   INPUT
;
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;
;       PIN LIST, RS-232C CONNECTION AS DATA TERMINAL EQUIPMENT. (DTE)
;       ALL CONNECTIONS TO J2, NO CONNECTIONS ALLOWED TO J1 OR J3.
;       USE THE FOLLOWING PARTS, OR EQUIVALENT IN THE CABLE ASSEMBLY:
;               CONNECTOR, FEMALE 232 PLUG      CINCH #  DB 25S
;               SHELL, PLUG                     CINCH #  DB 5126-1
;
;       PIN #   SIGNAL NAME                     IN/OUT
;
;       J2 - 1  FRAME GROUND
;       J2 - 7  SIGNAL GROUND
;       J2 - 20 DATA TERMINAL READY             OUTPUT
;       J2 - 5  CLEAR TO SEND                   INPUT
;       J2 - 2  TRANSMIT DATA                   OUTPUT
;       J2 - 8  CARRIER DETECT                  INPUT
;       J2 - 6  DATA SET READY                  INPUT
;       J2 - 4  REQUEST TO SEND                 OUTPUT
;       J2 - 3  RECEIVE DATA                    INPUT
;
;-----------------------------------------------
;
;       PIN LIST, RS-232C CONNECTION AS DATA COMMUNICATIONS EQUIPMENT. (DCE)
;       ALL CONNECTIONS TO J3, NO CONNECTIONS ALLOWED TO J1 OR J2.
;       USE THE FOLLOWING PARTS, OR EQUIVALENT IN THE CABLE ASSEMBLY:
;               CONNECTOR, MALE PLUG            MOLEX #  03-06-2151
;               PINS, MALE CRIMP   USE 15 EA.   MOLEX #  02-06-2103
;               SHELL, PLUG        USE 2 EA.    MOLEX #  15-04-0201
;
;       PIN #   SIGNAL NAME                     IN/OUT
;
;       J3 - 3  FRAME GROUND
;       J3 - 11 SIGNAL GROUND
;       J3 - 9  CLEAR TO SEND                   OUTPUT
;       J3 - 12 DATA SET READY                  OUTPUT
;       J3 - 15 CARRIER DETECT                  OUTPUT
;       J3 - 7  RECEIVE DATA                    OUTPUT
;       J3 - 6  DATA TERMINAL READY             INPUT
;       J3 - 14 TRANSMIT DATA                   INPUT
;
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;
;       PIN LIST, CURRENT LOOP CONNECTION. INPUT AND OUTPUT CURRENT
;       LEVELS (INCLUDING READER RUN SIGNAL) ARE 20 MA.
;       ALL CONNECTIONS TO J3, NO CONNECTIONS ALLOWED TO J1 OR J2.
;       EITHER INPUT OR OUTPUT LOOP MAY BE ACTIVE OR PASSIVE.
;       THE 20MA ENABLE SOURCE PIN MUST ALWAYS BE CONNECTED TO
;       THE 20MA ENABLE PIN BY A JUMPER IN THE EXTERNAL CONNECTOR.
;       TO CONNECT EITHER AN INPUT OR OUTPUT LOOP PAIR IN A PASSIVE
;       CONFIGURATION, USE THE (+) AND (-) SIGNALS, LEAVING THE
;       ASSOCIATED CURRENT SOURCE OPEN. TO CONNECT EITHER THE INPUT
;       OR OUTPUT LOOP PAIR IN AN ACTIVE CONFIGURATION, CONNECT
;       THE (-) SIGNAL TO GROUND WITH A JUMPER IN THE EXTERNAL
;       CONNECTOR, USE THE (+) SIGNAL AS THE (-) SIGNAL IN THE
;       EXTERNAL CABLE, AND USE THE ASSOCIATED CURRENT SOURCE AS
;       THE (+) SIGNAL IN THE EXTERNAL CABLE. NOTE THAT BOTH, ONE,
;       OR NONE OF THE TWO CURRENT LOOPS MAY BE ACTIVE OR PASSIVE.
;       THE READER RUN SIGNAL IS ALWAYS ACTIVE (20 MA. -> RUN)
;       USE THE FOLLOWING PARTS, OR EQUIVALENT IN THE CABLE ASSEMBLY:
;               CONNECTOR, MALE PLUG              MOLEX #  03-06-2151
;               PINS, MALE CRIMP   USE 15 EA.     MOLEX #  02-06-2103
;               SHELL, PLUG        USE 2 EA.      MOLEX #  15-04-0201
;
;       PIN #   SIGNAL NAME             PASSIVE NOTE    ACTIVE NOTE
;
;       J3 - 1  I LOOP ENABLE           JUMP TO PIN 4   JUMP TO PIN 4
;       J3 - 4  I LOOP ENABLE SOURCE    JUMP TO PIN 1   JUMP TO PIN 1
;
;       J3 - 2  (-) I LOOP OUT          (-) IN CABLE    JUMP TO PIN 3
;       J3 - 5  (+) I LOOP OUT          (+) IN CABLE    (-) IN CABLE
;       J3 - 6  OUTPUT CURRENT SOURCE   NO CONNECTION   (+) IN CABLE
;
;       J3 - 10 (-) I LOOP IN           (-) IN CABLE    JUMP TO PIN 11
;       J3 - 13 (+) I LOOP IN           (+) IN CABLE    (-) IN CABLE
;       J3 - 14 INPUT CURRENT SOURCE    NO CONNECTION   (+) IN CABLE
;
;       J3 - 9  (+) READER RUN
;       J3 - 8  (-) READER RUN
;
;       J3 - 3  SIGNAL GROUND
;       J3 - 11 SIGNAL GROUND
;
;-----------------------------------------------
;
;       DRAWING 800020, IN THE APPENDIX, PRESENTS A PIN DIAGRAM OF J3,
;       TYPICAL INTERFACE CIRCUITS, AND OTHER INFORMATION PERTINENT
;       TO THE CURRENT LOOP INTERFACE.
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;-----------------------------------------------
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SWITCHED CONTROL OF THE SERIAL INTERFACE FUNCTIONAL CHARACTERISTICS IS EXERCISED THRU SW1 AND SW2 (SEE FIG.1). THESE SWITCH BLOCKS CONTAIN SIXTEEN SWITCHES. THE DIRECTION OF SWITCHING TO THE ON OR OFF STATE MAY VARY, AND SHOULD BE CHECKED BEFORE SETTING THE SWITCHES. SWITCHES SHOULD NEVER BE CHANGED WHILE THE DATA PROCESSOR POWER IS ON. THE SWITCHES ARE REFERENCED BY NUMBERS S1 THRU S16, LEFT TO RIGHT. THEIR FUNCTIONS ARE AS FOLLOWS:

UNIT SELECTION...SWITCHES 1 THRU 4. THESE SELECT ONE OF EIGHT I/O ADDRESSES FOR THE CONTROL AND STATUS REGISTER, AND DATA REGISTER OF THE SERIAL INTERFACE. UNIT Ø OCCUPIES THE ADDRESSES NORMALLY USED AS THE CONSOLE TERMINAL FOR CONTROL OF THE OPERATING SYSTEM. THIS SHOULD BE SELECTED (NORMALLY) ONLY IF THE SERIAL IS TO BE USED TO INTERFACE THE CONSOLE TERMINAL. THE FOLLOWING TABLE COVERS THE SWITCH PATTERNS.

S1	S2	S3	S4	UNIT #	I/O REGISTER BASE ADDRESS	INTERRUPT VECTOR BASE ADDRESS
OFF	OFF	ON	ON	Ø	177560	6Ø
ON	OFF	ON	OFF	1	177520	12Ø
ON	OFF	OFF	OFF	2	177530	13Ø
OFF	OFF	OFF	OFF	3	177570	15Ø
ON	ON	ON	OFF	4	176520	32Ø
ON	ON	OFF	OFF	5	176530	33Ø
OFF	ON	ON	OFF	6	176560	34Ø
OFF	ON	OFF	OFF	7	176570	35Ø

CHARACTERISTICS SWITCHES...SWITCHES 5 THRU 8. THESE MAY BE SET TO ANY PATTERN. THE SETTING OF THESE SWITCHES WILL BE AVAILABLE IN BOTH THE RECEIVER STATUS REGISTER AND THE TRANSMITTER STATUS REGISTER OF THE SERIAL INTERFACE, TO BE USED AS REQUIRED BY THE I/O SOFTWARE. TYPICALLY, THESE WOULD IDENTIFY THE TYPE OF TERMINAL OR MODEM ATTACHED, OR CAN BE USED TO ENCODE A "STATION NUMBER" FOR CLUSTERS OF 8510 SYSTEMS.
NOTE THAT A SWITCH SET TO THE "OFF" POSITION GENERATES A "ONE" BIT IN BOTH STATUS REGISTERS (AND "ON" GENERATES "ZERO").

SWITCH #	BIT # (STATUS REGISTER)
5	11
6	10
7	9
8	8

NUMBER OF BITS...SWITCH 9. THIS SWITCH SELECTS THE NUMBER OF BITS USED IN THE SERIAL ASCII CODE, AS:

ON	7 BITS
OFF	8 BITS

PARITY ENABLE...SWITCH 10. THIS SWITCH ENABLES THE TRANSMISSION OF PARITY, OR THE TRANSMISSION OF A "SPACE" FOR THE PARITY BIT. ON INPUT, THIS SWITCH ALSO ENABLE THE VERIFICATION OF PARITY, SETTING AN ERROR CONDITION IF ENABLED.

ON	PARITY IS ACTIVE
OFF	PARITY DISABLED

TTY FILTER...SWITCH 11. THIS SWITCH CONNECTS THE NOISE FILTER FOR SUPPRESSION OF TRANSIENTS WHILE DRIVING AN ASR33 TYPE TELETYPEWRITER USING THE CURRENT LOOP INTERFACE. THIS SWITCH MUST BE OFF EXCEPT WHEN DRIVING SUCH A TERMINAL AT LOW DATA SPEEDS (TYPICALLY 110 BAUD).

ON	FILTER IS CONNECTED
OFF	FILTER DISCONNECTED

PARITY...SWITCH 12. THIS SWITCH IS ACTIVE ONLY IF PARITY IS ENABLED BY SWITCH 10. EVEN OR ODD PARITY FOR BOTH TRANSMISSION AND RECEPTION OF DATA IS SELECTED AS:

ON	ODD PARITY
OFF	EVEN PARITY

DATA RATE...SWITCHES 13 THRU 16. THESE SWITCHES SELECT ONE OF THE FOLLOWING FOURTEEN DATA RATES FOR BOTH TRANSMISSION AND RECEPTION OF DATA. THE TWO REDUNDANT CASES ARE INCLUDED.

S13	S14	S15	S16	DATA RATE, BAUD	
ON	ON	ON	OFF	50	
ON	ON	OFF	OFF	75	
OFF	OFF	OFF	OFF	110	
OFF	ON	ON	ON	134	
OFF	OFF	ON	OFF	150	
OFF	ON	OFF	ON	200	
OFF	OFF	OFF	ON	300	
OFF	ON	ON	OFF	600	
ON	OFF	OFF	OFF	1200	
ON	OFF	ON	OFF	1800	
OFF	ON	OFF	OFF	2400	
OFF	OFF	ON	ON	2400	(REDUNDANT)
ON	OFF	OFF	ON	4800	
ON	OFF	ON	ON	9600	
ON	ON	ON	ON	19200	
ON	ON	OFF	ON	19200	(REDUNDANT)

WITH THE SERIAL INTERFACE EIB SWITCHES SET CORRECTLY FOR THE EQUIPMENT TO BE INTEFACED, THE SERIAL IS PROGRAMMED INTERNALLY BY ADDRESSING THE FOUR I/O REGISTERS AT THE SEQUENTIAL WORD ADDRESSES STARTING AT THE "I/O BASE ADDRESS" FOUND IN THE UNIT NUMBER TABLE ABOVE. ALSO, THE INTERRUPT VECTOR ADDRESS PAIR (ADDRESS AND STATUS WORDS) OCCUPY FOUR WORD IN LOW MEMORY STARTING AT THE "VECTOR BASE ADDRESS" FOUND IN THE UNIT NUMBER TABLE ABOVE. THUS, UNIT 1 OCCUPIES FOUR ADDRESSES IDENTIFIED AS FOLLOWS:

EXAMPLE...UNIT #1

RECEIVER STATUS REGISTER (RSR)	177520
RECEIVER DATA BUFFER (RDB)	177522
TRANSMITTER STATUS REGISTER (XSR)	177524
TRANSMITTER DATA BUFFER (XDB)	177526

RECEIVER VECTOR ADDRESS	120 / 122
TRANSMITTER VECTOR ADDRESS	124 / 126

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;       RECEIVER STATUS REGISTER CONTAINS ERROR INFORMATION, THE SETTING
;       OF THE EIB CHARACTERISTICS SWITCHES, AND "DONE", "INTERRUPT
;       ENABLE", AND "READER RUN" BITS. THESE ARE DEFINED BELOW:
;
;       RECEIVER STATUS REGISTER BIT MAP
;       ALL BITS ARE READ-ONLY UNLESS OTHERWISE NOTED
;
;       BIT #   0   ] <----- READER RUN (WRITE ONLY)
;       BIT #   1   ]
;       BIT #   2   ]
;       BIT #   3   ]
;       BIT #   4   ]
;       BIT #   5   ]
;       BIT #   6   ] <----- INTERRUPT ENABLE (READ AND WRITE)
;       BIT #   7   ] <----- DONE BIT
;       BIT #   8   ] <-\\
;       BIT #   9   ] <- \\ CHARACTERISTICS
;       BIT #   10  ] <- // SWITCHES (EIB)
;       BIT #   11  ] <-//
;       BIT #   12  ] <----- OVERRUN ERROR
;       BIT #   13  ] <----- BREAK DETECTED
;       BIT #   14  ] <----- PARITY ERROR DETECTED
;       BIT #   15  ] <----- ERROR (INCLUSIVE OR OF BITS 14, 13, 12)
;
;       WHEN A CHARACTER IS RECEIVED, THE DONE BIT WILL BE SET,
;       INDICATING THAT THE DATA IS AVAILABLE IN THE RECEIVER DATA BUFFER.
;       ONLY THE LOW ORDER 7 BITS OF THE DATA BUFFER ARE VALID.
;       IF THE INTERRUPT ENABLE BIT HAS BEEN PREVIOUSLY WRITTEN
;       ON, AN INTERRUPT THRU THE RECEIVER VECTOR ADDRESS WILL BE REQUESTED.
;       IF AN ERROR CONDITION IS DETECTED, THE ERROR BIT AND THE DONE BIT
;       WILL BE SET, AND AN INTERRUPT REQUESTED, IF ENABLED. THREE ERROR
;       CONDITIONS ARE DETECTED:
;               OVERRUN - NEW DATA HAS BEEN RECEIVED AND PLACED INTO
;                         THE DATA BUFFER BEFORE THE PROCESSOR ACCEPTED
;                         THE PREVIOUS DATA. CURRENT DATA IS VALID.
;               BREAK   - THE SERIAL INPUT LINE WAS IN A CONTINUOUS
;                         "MARK" CONDITION. THIS IS USED SOMETIMES AS A
;                         REVERSE CHANNEL TO REQUEST DATA TRANSMISSION.
;                         IT CAN ALSO INDICATE AN OPEN LINE.
;               PARITY  - A PARITY ERROR WAS DETECTED ON THE RECEIVED DATA.
;
;       WHEN A CHARACTER IS RECEIVED, THE READER RUN BIT IS CLEARED.
;       WHEN THE READER RUN BIT IS SET ON, A LINE IN THE CURRENT LOOP
;       INTERFACE TO ASR33 TYPE TELETYPEWRITTERS WILL ENABLE THE BUILT-IN
;       PAPER TAPE READER TO READ ONE CHARACTER. TO READ PAPER TAPE
;       CONTINUOUSLY, THE READER RUN BIT MUST BE SET FOR EACH CHARACTER.
;
;       WHEN A SYSTEM RESET, POWER CYCLE, OR RESET INSTRUCTION OCCUR,
;       THE DONE BIT WILL BE CLEARED. IF THE INTERRUPT ENABLE BIT IS SET
;       WHILE THE DONE BIT IS CLEARED, NO IMMEDIATE INTERRUPT
;       WILL OCCUR. IF THE INTERRUPT ENABLE BIT IS SET WHILE THE DONE BIT
;       IS SET, AN IMMEDIATE INTERRUPT WILL BE REQUESTED.
;
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;
;       TRANSMITTER STATUS REGISTER CONTAINS ERROR INFORMATION, THE SETTING
;       OF THE EIB CHARACTERISTICS SWITCHES, AND "DONE", "INTERRUPT
;       ENABLE", AN BREAK TRANSMISSION CONTROL BITS. THESE ARE DEFINED BELOW:
;
;       TRANSMITTER STATUS REGISTER BIT MAP
;       ALL BITS ARE READ-ONLY UNLESS OTHERWISE NOTED
;
;       BIT #   0   ] <----- TRANSMIT CONTINUOUS BREAK (WRITE ONLY)
;       BIT #   1   ]
;       BIT #   2   ]
;       BIT #   3   ]
;       BIT #   4   ]
;       BIT #   5   ]
;       BIT #   6   ] <----- INTERRUPT ENABLE (READ AND WRITE)
;       BIT #   7   ] <----- DONE BIT
;       BIT #   8   ] <-\\
;       BIT #   9   ] <- \\ CHARACTERISTICS
;       BIT #   10  ] <- // SWITCHES (EIB)
;       BIT #   11  ] <-//
;       BIT #   12  ]
;       BIT #   13  ]
;       BIT #   14  ]
;       BIT #   15  ] <-----ON -> MODEM READY
;
;       A CHARACTER IS TRANSMITTED WHEN THE TRANSMITTER DATA BUFFER IS
;       WRITTEN. TRANSMISSION IS CONSIDERED COMPLETE WHEN THE SERIAL
;       BIT STREAM HAS BEEN COMPLETELY GENERATED. THEN, THE DONE BIT
;       WILL BE SET, INDICATING THAT THE TRANSMITTER CAN ACCEPT ANOTHER
;       CHARACTER. ONLY THE LOW ORDER 7 BITS OF THE DATA BUFFER ARE VALID.
;       IF THE INTERRUPT ENABLE BIT HAS BEEN PREVIOUSLY WRITTEN ON,
;       AN INTERRUPT THRU THE TRANSMITTER VECTOR ADDRESS WILL BE
;       REQUESTED. THE MODEM READY BIT IS THE REVERSE LOGIC OF THE
;       RECEIVER ERROR BITS: ON SAYS THE MODEM IS READY. THIS BIT
;       DOES NOT GENERATE AN INTERRUPT. IT IS GENERALLY A STATIC
;       INDICATION THAT A MODEM IS PRESENT AND CONNECTED TO THE SERIAL
;       INTERFACE.
;
;       THE "TRANSMIT CONTINUOUS BREAK" BIT, WHEN SET ON, WILL
;       DO JUST THAT. THIS IS USED TO INDICATE AN INACTIVE STATE TO
;       THE RECEIVER OF THE TRANSMITTED DATA. THE BREAK STATE WILL BE
;       CONTINUOUS UNTIL THE BIT IS CLEARED OFF.
;
;       WHEN A SYSTEM RESET, POWER CYCLE, OR RESET INSTRUCTION OCCUR,
;       THE DONE BIT WILL BE SET. IF THE INTERRUPT ENABLE BIT IS SET
;       WHILE THE DONE BIT IS CLEARED, NO IMMEDIATE INTERRUPT
;       WILL OCCUR. IF THE INTERRUPT ENABLE BIT IS SET WHILE THE DONE BIT
;       IS SET, AN IMMEDIATE INTERRUPT WILL BE REQUESTED.
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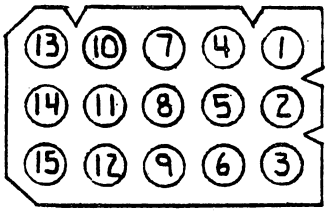
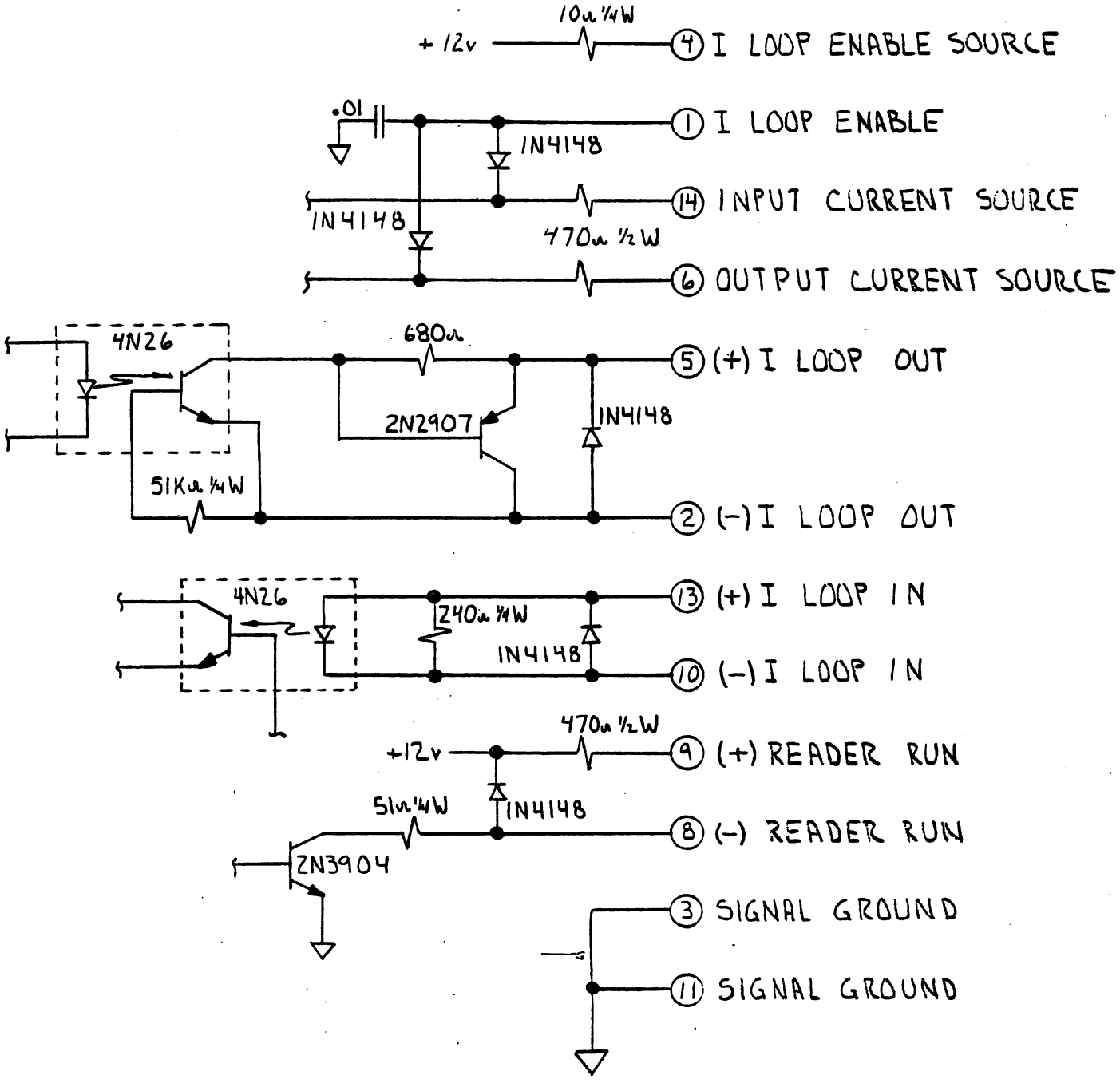


J3 VIEWED FROM REAR OF 8510

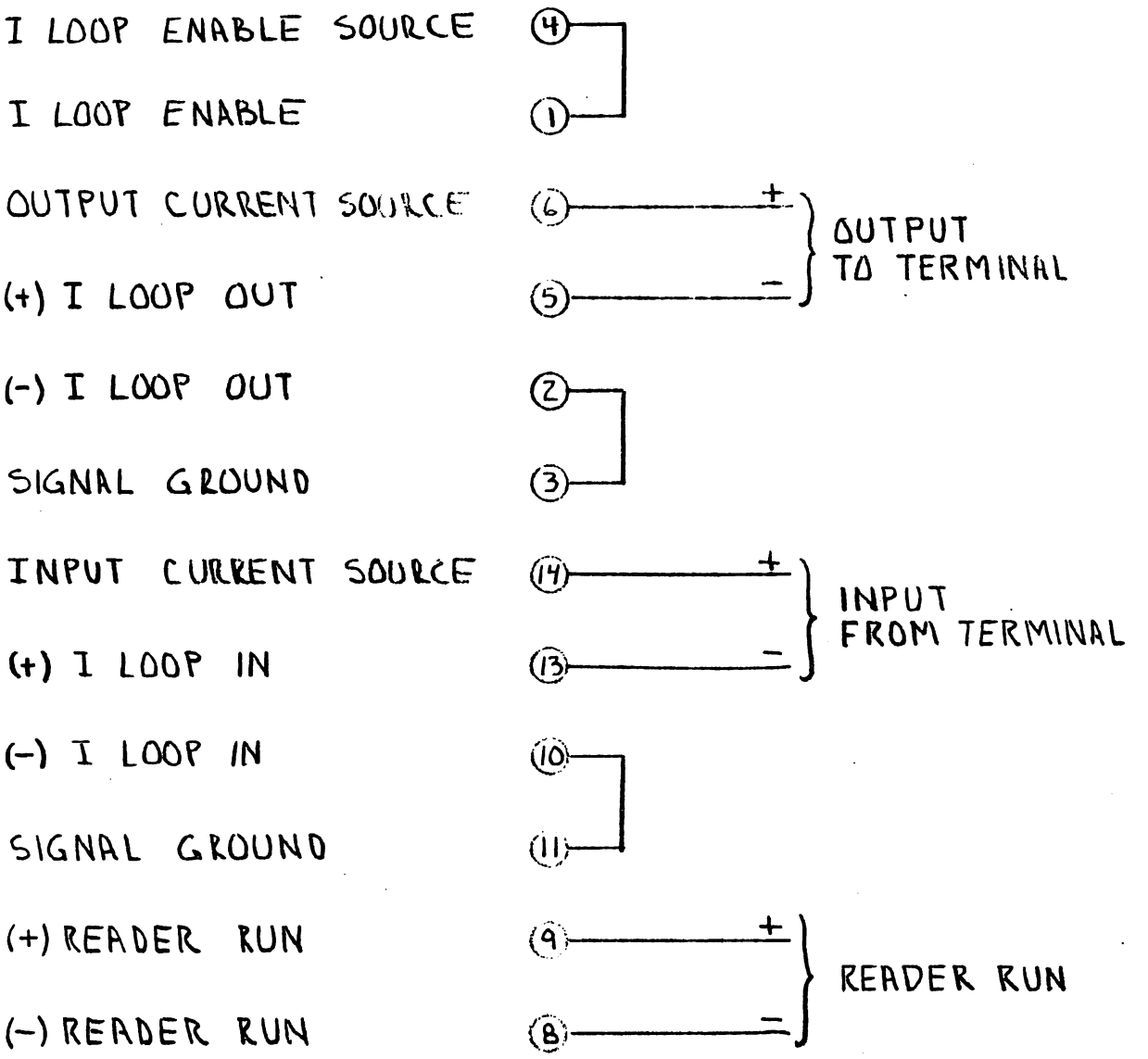
J3 PIN	DESCRIPTION		INPUT OUTPUT	EIA CKT	EIA PIN
	CURRENT LOOP	EIA RS-232-C AS DCE			
1	I LOOP ENABLE				
2	(-) I LOOP OUT				
3	SIGNAL GROUND	FRAME GROUND		AA	1
4	I LOOP ENABLE SOURCE				
5	(+) I LOOP OUT				
6	OUTPUT CURRENT SOURCE	DATA TERMINAL READY	I	CD	20
7		RECEIVED DATA	O	BB	3
8	(-) READER RUN				
9	(+) READER RUN	CLEAR TO SEND	O	CB	5
10	(-) I LOOP IN				
11	SIGNAL GROUND	SIGNAL GROUND		AB	7
12		DATA SET READY	O	CC	6
13	(+) I LOOP IN				
14	INPUT CURRENT SOURCE	TRANSMITTED DATA	I	BA	2
15		DATA CARRIER DETECT	O	CF	8

EIA -
POSITIVE VOLTAGE EQUALS BINARY ZERO, SPACE, ON
NEGATIVE VOLTAGE EQUALS BINARY ONE, MARK, OFF

800020
TERAK CORPORATION
8510 SINGLE SERIAL
J3 CONNECTOR
BRIAN J. BENZAR
5-18-76 4-25-78
SHEET 1 OF 4 REV B

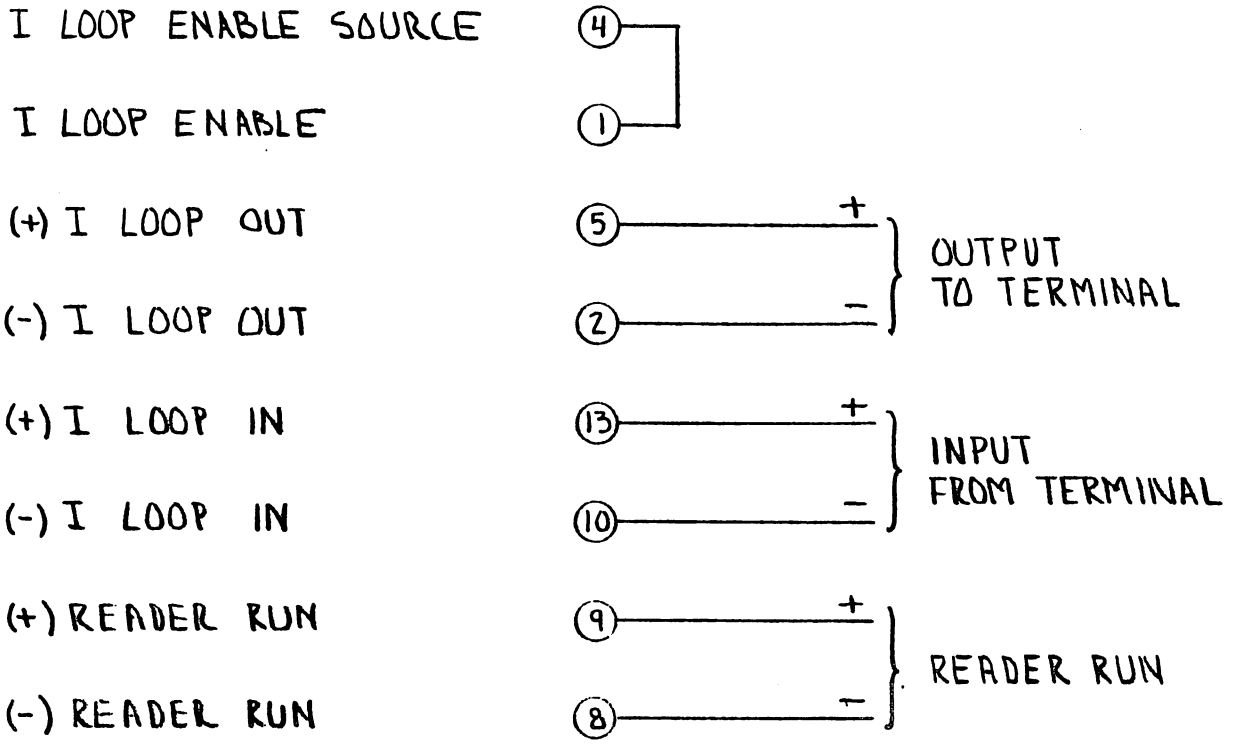


800020
TERAK CORPORATION
8510 SINGLE SERIAL
CURRENT LOOP INTERFACE
BRIAN J. BENZAR
5-18-76 4-25-78
SHEET 2 OF 4 REV B



FULL DUPLEX CURRENT LOOP INTERFACE
ACTIVE CONFIGURATION
(8510 SUPPLIES CURRENT SOURCE)

800070
TERAK CORPORATION
8510 SINGLE SERIAL
ACTIVE CURRENT LOOP CONF
BRIAN J. BENZAR
5-18-76 4-25-78
SHEET 3 OF 4 REV B



FULL DUPLEX CURRENT LOOP INTERFACE
PASSIVE CONFIGURATION
(TERMINAL SUPPLIES CURRENT SOURCE)

B0002O
TERAK CORPORATION
8510 SINGLE SERIAL
PASSIVE CURRENT LOOP CONF
BRIAN J. BENZAR
5-18-76
4-25-78
SHEET 4 OF 4
REV B